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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/755,465 | 01/13/2004 | Soo-Young Kim | 8947-000069/US | 9923 |

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| EXAMINER | |
|---|---|
| LE, THONG QUOC | |
| **ART UNIT** | **PAPER NUMBER** |
| 2827 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 04/25/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/755,465 | KIM, SOO-YOUNG | |
| | Examiner | Art Unit | |
| | Thong Q. Le | 2827 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-25* is/are allowed.

6)☒ Claim(s) *1,2,5,6,26,27,30-35 and 39-41* is/are rejected.

7)☒ Claim(s) *3-4,7,28-29,36-38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Amendment filed on 02/12/2007 has been entered.

2. Claims 1-41 are presented for examination.

### *Response to Arguments*

3. Applicant's arguments with respect to claims 1-41 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Objections*

4. Regarding claim 34, line 4, should be changed "**section** refresh section" to –**second** refresh section--.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-2, 5-6, 26-27, 30-35, 39-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Takahashi et al. (Pub. U.S. Patent No. 2004/0130958).

Regarding claim1, Takahashi et al. disclose a semiconductor memory device (Figure 1), comprising:

an oscillator circuit (Figure 23, 811, [0180])for generating an oscillation signal that varies based on a mode of operation ([0174], Figure 22, [0178-0182], Figure 24, oscillation signal is switched between active mode and stand-by mode);

a word line enable circuit (Figure 11) for generating a word line enable signal (Figure 11, RE, ABSTRACT) in response to the oscillation signal ([0015]); and

a control circuit (Figure 1, 8A, 8B, 8C, 9, 10, 14, [0030], *control system circuits*) for controlling the oscillator circuit and the word line enable circuit so that a pulse width of the word line enable signal is widened as operation mode of the memory device changes from an active mode to a stand-by mode ([0028-0030]).

Regarding claim 2, Takahashi et al. disclose wherein a period of the oscillation signal is maintained as operation mode changes due to the widening of the pulse width ([0029]).

Regarding claim 5, Takahashi et al. disclose wherein the period of the oscillation signal is equal to a refresh period ([0024], [0028]).

Regarding claim 6, Takahashi et al. disclose wherein the control circuit controls the refresh period and the pulse width of the word line enable signal in response to a

chip select signal (Figure 1, /CS, [0066-0067]), and wherein the pulse width of the word line enable signal is maintained equally during a refresh section of the stand-by mode (Figure 7, REF).

Regarding claims 26-27, Takahashi et al. disclose a method of operating a semiconductor memory device having an active mode of operation and a stand-by mode of operation, comprising:

generating a flag signal (Figure 1, 2, [0083], signal SATD) indicating an end of a first refresh section of the stand-by mode ([0014], [0071]); generating an oscillation signal (Figure 23, CK0) in response to the flag signal; and generating a word line enable signal (Figure 12, RE) in response to the oscillation signal, the word line enable signal having a pulse width that varies depending on the mode of operation of the device (Figure 10), and wherein the flag signal has an inactive period and an active period, the inactive period of the flag signal includes the active mode and the first refresh section of the stand-by mode, and the active period of the flag signal includes a second refresh section of the stand-by mode of operation ([0070]).

Regarding claim 30, Takahashi et al. disclose a control circuit (Figure 1) for a semiconductor memory device, the device having an oscillation circuit (Figure 23) for generating an oscillation signal (Figure 23, CK0) and a word line enable circuit for generating a word line enable signal (Figure 11, RE) in response to the oscillation signal, the control circuit comprising:

a buffer circuit (Figure 1, 8A) ; and

a detector circuit (Figure 1, 2) , wherein the buffer circuit outputs a chip select signal (Figure 1, /CS) to the detector circuit and the word line enable circuit, and the detector circuit generates a flag signal ([0070], SATD) for controlling the oscillation circuit based on a detection of a change in operation mode of the device ([0070-0071]).

Regarding claim 31, Takahashi et al. disclose wherein the oscillation signal varies based on mode of operation of the device (Figure 24).

Regarding claim 32, Takahashi et al. disclose wherein the buffer circuit and detector circuit control the oscillating circuit so that a period of the oscillation signal is maintained for a given period of time as the device changes mode of operation (Figure 22, CK0, /CS, stand-by and active modes).

Regarding claim 33, Takahashi et al. disclose wherein the buffer circuit and detector circuit control the word line enable circuit so that a pulse width of the word line enable signal is widened as the device changes from an active mode of operation to a stand-by mode of operation ([0082-0085]).

Regarding claim 34, Takahashi et al. disclose wherein the device has an active mode of operation and a standby-mode of operation, and the stand-by mode of operation spans a duration that includes at least two periods of time, represented as a first refresh section and a section refresh section (Figure 22).

Regarding claim 35, Takahashi et al. disclose wherein the flag signal ([0083], SATD) has an inactive period and an active period, the inactive period of the flag signal includes the active mode and the first refresh section of the stand-by mode, and the active period of the flag signal includes the second refresh section ([0083]).

Regarding claims 39-41, Takahashi et al. disclose a method of controlling operation of a semiconductor memory device ([0036-0037]) that includes a control circuit ([0015]) for controlling an oscillation circuit and a word line enable circuit (Figure 11, [0015]), the method comprising:

controlling a length of a period of the oscillation signal generated ([0030-0032]) by the oscillation circuit and a pulse width of a word line enable signal generated by the word line enable circuit (Figure 11, RE) in response to the oscillation signal based on a change in mode of operation of the device, and the pulse width of the word line enable signal being widened based on the change in the mode of operation of the device (Figure 13, Figure 22).

***Allowable Subject Matter***

7. Claims 3-4, 7, 28-29, 36-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-4, 7, 28-29, 36-38 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Takahashi et al. (Pub. U.S. Patent No. 2004/0130958), and others, does not teach the claimed invention having a wherein the control circuit controls the oscillator circuit so that the period of the oscillation signal is lengthened after a given time elapses from the beginning of the stand-by mode.

8. Claims 8-25 are allowed.

Claims 8-25 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Takahashi et al. (Pub. U.S. Patent No. 2004/0130958), and others, does not teach the claimed invention having a flag signal generator circuit for generating a flag signal indicating an end of a first refresh section of a stand-by mode of operation, after a given time elapses from a start of the stand-by mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le
Primary Examiner
Art Unit 2827